1. A method of fabricating complementary metal oxide semiconductor (CMOS) devices on a semiconductor substrate, featuring a silicon - germanium (SiGe), layer used as a component of a CMOS device channel region, with the integration of a selective epitaxially deposited, strained SiGe channel layer in a CMOS process performed after formation of isolation regions, comprising the steps of:

providing a first region of said semiconductor substrate to be used as an NMOS (N channel metal oxide semiconductor) region, and providing a second region of said semiconductor substrate to be used as a PMOS (P channel metal oxide semiconductor) region;

forming isolation regions in top portions of said semiconductor substrate;

forming a P well region in said NMOS region, and forming an N well region in said PMOS region;

selectively depositing a composite silicon layer on the top surface of portions of said semiconductor substrate not occupied by said isolation regions, with said composite silicon layer comprised of said SiGe layer, and comprised of an overlying silicon layer; and

forming a gate insulator layer on said overlying silicon layer.

2. The method of claim 1, wherein said isolation regions are insulator filled, shallow trench isolation regions.

3. The method of claim 1, wherein said composite silicon layer is an undoped composite silicon layer.

4. The method of claim 1, wherein said SiGe layer is grown on an underlying silicon layer.

5. The method of claim 1, wherein silicon layer, underlying said SiGe layer, is obtained at a thickness between about 0 to 100 Angstroms.

6. The method of claim 1, wherein silicon layer, underlying said SiGe layer, is selectively grown via ultra-high vacuum chemical vapor deposition (UHV - CVD) procedures.

7. The method of claim 1, wherein silicon layer, underlying said SiGe layer, is selectively grown at temperature between about 400 to 800° C, and at a pressure between less than 200 mtorr, using silane or disilane as a source.

8. The method of claim 1, wherein said SiGe layer of said composite silicon layer, is selectively grown to a thickness between about 20 to 150 Angstroms, with a germanium content between about 20 to 40 weight percent..

9. The method of claim 1, wherein said SiGe layer is selectively grown via ultra-high vacuum chemical vapor deposition (UHV - CVD) procedures.

10. The method of claim 1, wherein said SiGe layer is selectively grown at a temperature between about 400 to 800° C, and at a pressure less than 200 mtorr, using silane or disilane, and germane as reactants.

11. The method of claim 1, wherein said overlying silicon layer of said composite silicon layer, is selectively grown to a thickness between about 5 to 100 Angstroms.

12. The method of claim 1, wherein said overlying silicon layer is selectively grown via ultra-high vacuum chemical vapor deposition (UHV - CVD) procedures.

13. The method of claim 1, wherein said overlying silicon layer is selectively grown at a temperature between about 400 to 800° C, and at a pressure less than 200 mtorr, using silane or disilane as a source.

14. The method of claim 1, wherein said gate insulator layer is a silicon dioxide gate insulator layer.

15. The method of claim 1, wherein said gate insulator layer is obtained at a thickness between about 5 to 80 Angstroms, via thermal oxidation procedures performed at a temperature between about 600 to 900° C, in an oxygen - steam ambient.

16. A method of forming CMOS devices featuring a channel region formed in a selectively grown, composite silicon layer, wherein said composite silicon layer is comprised of at least a strained SiGe layer and an overlying silicon layer, comprising the steps of:

providing a first region of said semiconductor substrate to be used as an NMOS region, and providing a second region of said semiconductor substrate to be used as a PMOS region;

forming shallow trench isolation (STI) regions in top portions of said semiconductor substrate, with a top portion of each STI region featuring tapered sides;

forming a P well region in a top portion of said NMOS region, and forming an N well region in a top portion of said PMOS region;

selectively depositing a composite silicon layer on the top surface of said P well region and on the top surface of said N well region, with said composite silicon layer featuring tapered sides, resulting in V-groove openings located between said tapered sides of said STI regions and tapered sides of said composite silicon layer, and with said composite silicon layer comprised of a silicon layer, a strained SiGe layer, and an overlying silicon layer;

depositing an insulator layer;

removing portion of insulator layer from the top surface of said composite insulator layer resulting in insulator filled V-grooves located between said STI regions and said composite silicon layer; and

thermally oxidizing a top portion of said overlying silicon layer to form a silicon dioxide gate insulator layer on a bottom portion of said overlying silicon layer.

17. The method of claim 16, wherein said STI regions are silicon oxide filled shallow trench shapes, formed to a depth between about 3000 to 6000 Angstroms in said semiconductor substrate.

18. The method of claim 16, wherein said composite silicon layer is obtained via ultra-high vacuum chemical vapor deposition (UHV - CVD) procedures, at a temperature between about 400 to 800° C, and at a pressure less than 200 mtorr.

19. The method of claim 16, wherein said SiGe layer is grown on an underlying silicon layer.

20. The method of claim 16, wherein said silicon layer of said composite silicon layer, underlying said SiGe layer, is selectively grown to a thickness between about 0 to 100 Angstroms, using silane or disilane as a source.

21. The method of claim 16, wherein said strained SiGe layer of said composite silicon layer, is selectively grown to a thickness between about 20 to 150 Angstroms.

22.The method of claim 16, wherein said strained SiGe layer of said composite silicon layer, is selectively grown with a germanium content between about 20 to 40 weight percent.

23.The method of claim 16, wherein said strained SiGe layer of said composite silicon layer, is selectively grown using silane or disilane, and germane as reactants.

24. The method of claim 16, wherein said overlying silicon layer of said composite silicon layer, is selectively grown to a thickness between about 5 to 100 Angstroms using silane or disilane as a source.

25. The method of claim 16, wherein said insulator layer, used to fill said V-groove openings, is a silicon oxide layer, obtained via deposition of a silicon oxide layer at a thickness between about 100 to 1000 Angstroms.

26. The method of claim 16, wherein removal of said insulator layer used to form said insulator filled V- grooves, is accomplished via reactive ion etching procedures.

27. The method of claim 16, wherein said silicon dioxide gate insulator layer is obtained at a thickness between about 5 to 80 Angstroms, via thermal oxidation procedures performed at a temperature between about 600 to 900° C, in an oxygen - steam ambient.